CASE STUDY

Managing Conflicting KPIs in the Diffusion Area at Renesas Electronics Using Multi-objective Optimization

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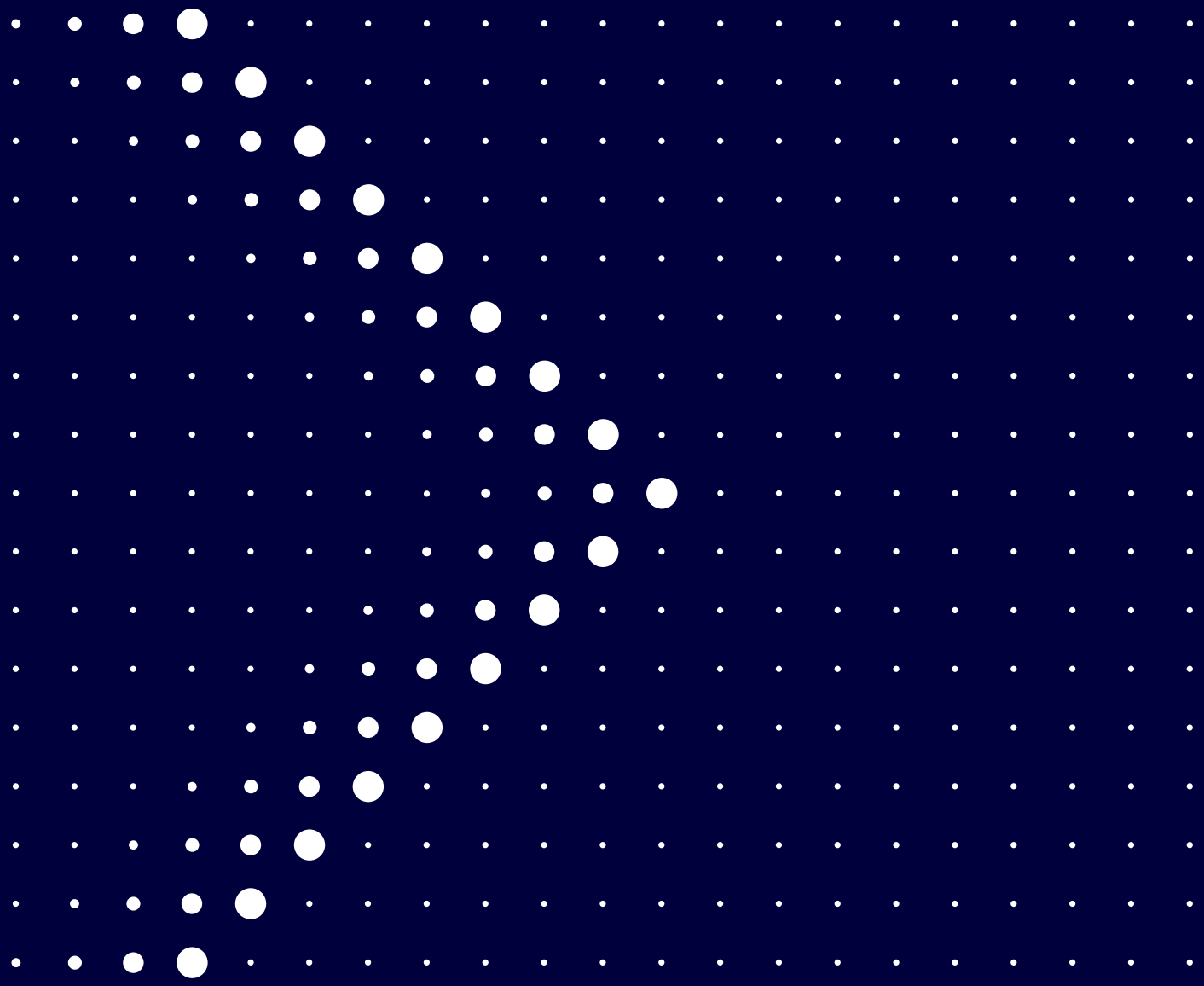


Flexciton

Managing three conflicting KPIs with multi-objective optimization

The Challenge

Renesas Electronics is a global leader in microcontrollers, analog, power, and SoC products, providing comprehensive solutions to a range of industries from automotive to consumer electronics. The Japanese manufacturer's US wafer fab specialises in manufacturing high-performance industrial and analog integrated circuits.

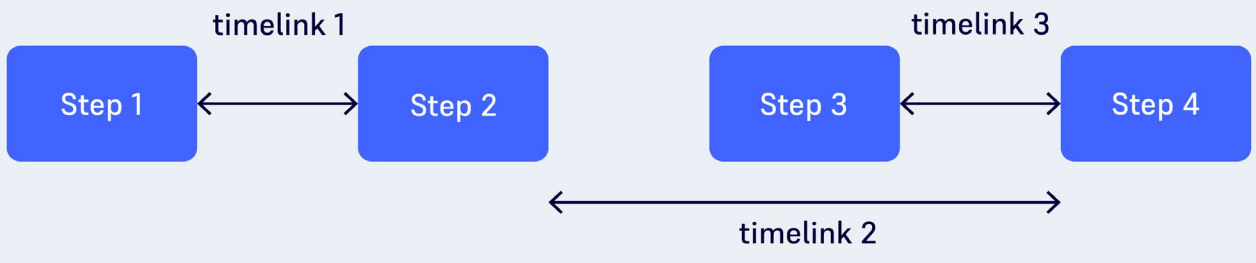
Renesas were interested to see how optimization-based technology could be applied to specific toolsets in their US facility, specifically those in the diffusion area. They had the objective of decreasing the number of batches (increasing batch sizes) and decreasing cycle time across this area of the fab. This is difficult to achieve in a scheduling sense as there is a conflicting trade-off between batch size and queue time, a key component to minimising cycle time.

Usually, operators manually batch wafers to the best of their ability with the limited information they have available, such as which lots are currently queuing, but it is incredibly difficult for a human to make decisions that take into account the lots that will arrive in the future. Without knowledge of the arrival times of future lots, operators can unnecessarily wait to maximise a batch size, causing more lots to queue and damaging productivity.

Timelink constraints, also referred to as time lag constraints, time loops, qtime, or close coupling constraints, are another difficult trade-off that defines the diffusion area. Timelink constraints are designed to eliminate queuing time at subsequent steps and refer to a maximum elapsed time a lot can spend between two or more process steps. They are critical to helping minimise the risk of oxidation or contamination that can take place when a wafer is queuing outside of a tool for too long, which risks wafer scrappage or rework that damages a fab's profitability.

Figure 1 shows an example of how timelinks can also conflict with batching and queue time. Because of the overlapping timelinks (timelink 2 and timelink 3), if step 3 is scheduled too close to step 2 it may make timelink 3 impossible to meet. This is because the time between steps 3 and 4 is greater than the maximum allowed before the lot could become contaminated. To avoid timelink violations like this, a fab needs the ability to look ahead to consider future decisions whilst also being constrained by past decisions. This phenomenon makes timelink constraints one of the most challenging aspects of

Figure 1 shows an example timelink system between four consecutive steps. The overlapping timelinks mean that after completing step 3, the lot begins a new timelink (3) whilst still transitioning an existing timelink (2).



a wafer fab to schedule, which makes solving them using conventional heuristic approaches unfeasible.

The Solution

Managing the conflicting objectives whilst increasing the efficiency of the diffusion area requires a multi-objective optimization approach to scheduling. To demonstrate how Flexciton's intelligent scheduling platform can handle such a problem, Renesas provided us with real-world historical datasets from their diffusion area.

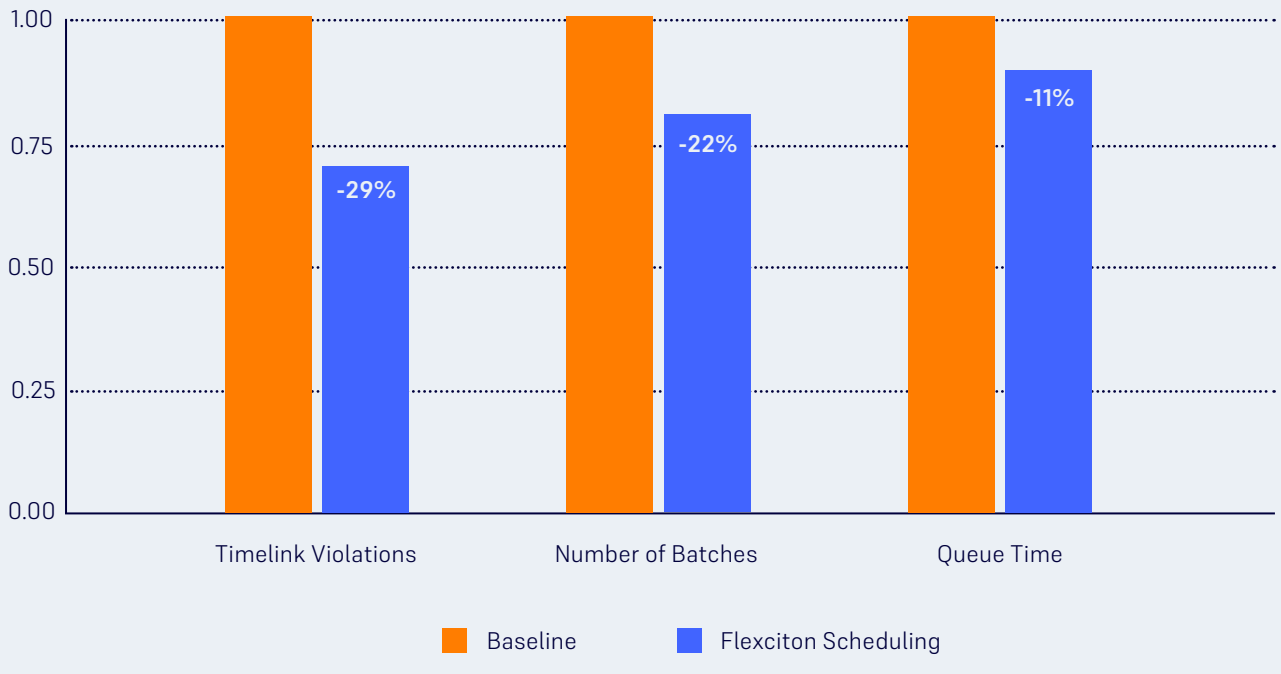
Flexciton's solution for solving global scheduling problems consists of a hybrid of mixed-integer linear programming (MILP) models and heuristics. This approach can be broken down into two stages: constructive and improvement. The constructive step quickly produces a high-quality schedule within 2-3 minutes. To do this, we identify bottleneck toolsets and then rank all lots according to a combination of criteria that includes due date, timelink constraints, and number of steps.

Once we have a high-quality schedule, the improvement step then carefully refines it for a further 2-3 minutes. It explores possibilities by shuffling lots around within a close proximity of their position in the schedule to find the best quality solution. When solving any one toolset, we are considering the knock-on impact of making one change against all the other toolsets in the schedule. This global view of the fab is one of the reasons why we have found our solution to outperform conventional heuristic approaches. The process of iteration continues until we have found an optimal solution for all toolsets or the chosen time limit has exhausted.

Results

To put our technology to the test using real-world historical data from the diffusion area at Renesas, we packaged the solution inside a simulation environment that replicates the way Flexciton's scheduler operates in a live fab. This means that information that would be uncertain in a live

Figure 2 shows the KPI improvements for timelink violations, number of batches, and queue time against the baseline results.



environment is withheld from the scheduler which it must estimate itself in turn. From this, we were able to prove impressive gains on the conflicted KPIs that Renesas had targeted. Timelink violations at the diffusion area were reduced by a significant 29% whilst simultaneously, the number of batches and queue time were reduced by 22% and 11%, respectively (Figure 2). These results demonstrate how Flexciton's technology is able to manage even the most complex of scheduling scenarios and maximise a fab's productivity and profitability.

About Flexciton

Flexciton provides solutions for semiconductor manufacturers to power their transition towards autonomous factories. Our intelligent planning and scheduling software suite combines advanced optimisation techniques with the power of AI to orchestrate complex fab workflows and achieve critical revenue-to-shop-floor alignment.

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About Renesas

A global leader in microcontrollers, analog, power, and SoC products, Renesas provides comprehensive solutions for a broad range of automotive, industrial, home electronics, office automation, and information communication technology applications that help shape a limitless future.

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